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ABSTRACT OF THE DISCLOSURE

MAPPING TEST MUX STRUCTURE

5 A method and apparatus for observing the state of signals during chip testing. For a chip
containing many instances of the same module, it is advantageous to observe the same signal set
for several of the modules concurrently. In particular, the present invention improves upon prior
test MUX methods by placing additional mapping/steering logic within a module to provide
greater flexibility in selecting signal sets for concurrent observation. The addition of
10 mapping/steering logic to a module's test MUX structure allows a chip designer to arbitrarily
map each of the test signal groups to any of the test output groups.